## ABSTRACT

An array capacitor is described for use with an integrated circuit (IC) mounted on an IC package. The array capacitor includes a number of first conductive layers interleaved with a number of second conductive layers and a number of dielectric layers separating adjacent conductive layers. The array capacitor further includes a number of first conductive vias to electrically connect the first conductive layers and a number of second conductive vias to electrically connect the second conductive layers. The array capacitor is provided with openings which are configured to enable pins from an IC package to pass through.